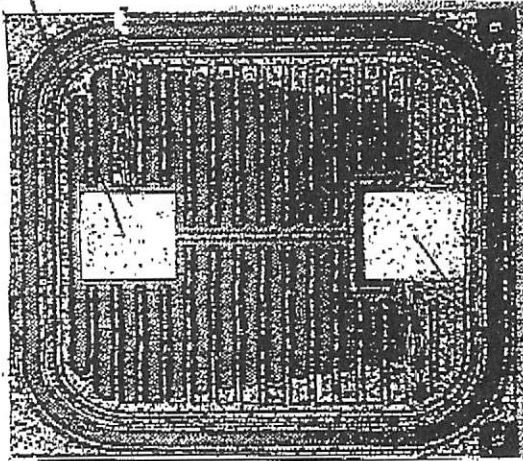


Daniel Olsen

Sierra

DIE TECHNOLOGY LIMITED

GATE

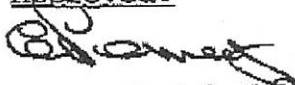


SOURCE

CHIP BACK IS DRAIN

NOTE: This geometry is numbered G21 in the Zetex Silicon Services and Semiconductor Dice Technical Handbook 1991. It has been numbered G25 in other publications.

The information on this layout is believed to be correct. No liability for error or omission can be accepted. The supply of dice to this layout can only be guaranteed if it forms part of a specification or the chip identification, if below, is requested. Chip back potential is the level at which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated above. If no potential is given the chip back should be isolated. Nominal metal thicknesses are based on manufacturer's information.

<u>Approved:</u>  <u>Date:</u> 7-12-93	<u>Metallisation/Thickness(KA)</u> Top : Al 12 Back: Au 15 Back Potential: Drain Man's. Part No:	<u>Chip Identification</u> Line Source: Mask Ref : See Process : NOTE Version : above Geometry : G21
Corbrook Road Chadderton Lancs. OL9 9SD Tel: 061 626 3827 Fax: 061 627 2341	<u>Dimensions (mils.):</u> 30 x 30 x 10 ZETEX BSS123	<u>Bond Pads:</u> 5 x 5 Issue 1